What is claimed is:

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1. A processor comprising:

at least one register file;

at least one execution unit;

said at least one register file operatively connected to said at least one execution unit; and,

a backing register file operatively coupled to said at least one register file, and where said backing register file is operationally and responsively coupled to at least one user-visible instruction.

2. A processor as in claim 1 further comprising a plurality of register files and further comprising at least one execution unit operably connected to each register file of said plurality of register files, and where said backing register file is operably connected to each of said plurality of register files providing thereby the ability to transfer values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files.

3. A processor as in claim 1 further comprising a connection circuit having a first connection and a second connection, where said first connection is

operably connected to said backing register file and said second connection is operably connected to a main memory.

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4. A processor as in claim 2 further comprising a connection circuit having a first connection and a second connection, where said first connection is operably connected to said backing register file and said second connection is operably connected to a main memory.

5. A method for moving values from designated locations in designated register files to designated locations in a backing register file and values in designated locations in said backing register file to designated locations in designated register files comprising:

(a) identifying a backing register file instruction in a sequence of instructions;

(b) decoding said backing register file instruction, making available addresses for specified numbers of locations in specified register files and an equal number of addresses for specified locations in said backing register file, where said number of addresses is at least one, where if said backing file instruction is one of load-backing-register-file or load-register-file;

(c) reading values from each of said addresses in said specified register file and writing said values to said equal number of addresses in said backing register

file as specified by said backing register file instruction, if said backing register file instruction is of type load-backing-register-file; and,

(c) reading values from each of said addresses specified in said backing register file and writing said values to said equal number of addresses in said specified register file, if said backing register file instruction is of type load-register-file.

6. A method for moving values from designated locations in main memory to designated locations in a backing register file and values in designated locations in said backing register file to designated locations in main memory comprising:

(a) identifying a backing register file instruction in a sequence of instructions;

(b) decoding said backing register file instruction, making available addresses for specified numbers of locations in main memory and an equal number of addresses for specified locations in said backing register file, where said specified number of locations is at least one, if said backing register file instruction is one of load-main-memory or load-register-backing-file;

(c) reading values from each of said addresses in said main memory and writing said values to said equal number of addresses in said backing register file as specified by said backing register file instruction, if said backing register file instruction is of type load-backing-register-file; and,

(c) reading values from each of said addresses specified in said backing register file and writing said values to said equal number of addresses in said main memory as specified by said backing file instruction, if said backing register file instruction is of type load-backing-register-file.

7. A machine readable medium containing a data structure having a backing register file instruction therein.

8. A machine readable medium containing a data structure as in claim 7 further comprising a backing register file instruction for transferring register values between a register file and said backing register file.

9. A machine readable medium containing a data structure as in claim 7 further comprising a backing register file instruction for transferring values between main memory and said backing register file.